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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/261,328	03/03/1999	THOMAS G. FERENCE	BU9-98202	7631

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EXAMINER

GRAYBILL, DAVID E

ART UNIT	PAPER NUMBER
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2814

DATE MAILED: 12/11/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/261,328

Applicant(s)

FERENCE ET AL.

Examiner

David E Graybill

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 05 November 2001.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-59 is/are pending in the application.
- 4a) Of the above claim(s) 7-9, 19, 21-24 and 26-53 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6, 10-18, 20, 25 and 54-59 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 November 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

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A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11-05-01 has been entered.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 55-59 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 55 the limitation, "the plurality of first solder bumps are free of connection with any of the plurality of contacts" is ambiguous and appears to be incompatible with the claim 55 limitation, "first solder bumps connected between the first substrate and the second substrate" because the second limitation appears to encompass at least indirect connection between the first bumps and the contacts via the substrates.

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The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-6, 17, 18, 20, 25, 54-57 and 59 are rejected under 35 U.S.C. 102(b) as being anticipated by Nishiguchi (5214308).

1. A semiconductor structure, comprising: a first substrate 3; a second substrate 1 joined to the first substrate; a plurality of contacts 2b between the first substrate and the second substrate; and a plurality of first solder bump 2a connected between the first substrate and the second substrate which align the plurality of contacts, wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of contacts.

3. The semiconductor structure according to 1, wherein at least one of the first substrate and the second substrate is an integrated circuit chip.

4. The semiconductor structure according to 1, wherein the contacts comprise second solder bumps.

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5. The semiconductor structure according to 4, wherein the second solder bumps have a smaller size than the first solder bumps.

6. The semiconductor structure according to 1, wherein the contacts have a smaller size than the first solder bumps.

17. The semiconductor structure according to 1, wherein an upper surface of the contacts and an upper surface of the first solder bumps are co-planar.

18. The semiconductor structure according to 1, further comprising: a ledge on at least one of the first substrate and the second substrate, wherein the first solder bumps are arranged in contact with the ledge, such that an upper surface of the contacts and an upper surface of the first solder bumps are co-planar.

20. The semiconductor structure according to 1, wherein the contacts comprise solder.

25. The semiconductor structure according to 1, wherein at least one of the first substrate and the second substrate is an integrated circuit chip, and the contacts are sufficiently small to permit alignment of individual devices on the integrated circuit chips.

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54. The semiconductor structure of 1, wherein the plurality of first solder bumps align a plurality of controlled collapse chip connection contacts 2b.

55. A semiconductor structure, comprising: a first substrate; a second substrate opposing the first substrate; a plurality of contacts between the first substrate and the second substrate; and a plurality of first solder bumps connected between the first substrate and the second substrate which align the plurality of contacts, wherein the plurality of first solder bumps are free of connection with any of the plurality of contacts.

56. The semiconductor structure of 55, wherein the plurality of first solder bumps are arranged around a periphery of an area containing the plurality of contacts.

57. The semiconductor structure of 55, wherein the plurality of first solder bumps align a plurality of controlled collapse chip connection contacts.

58. The semiconductor structure of 55, further comprising a ledge on the first substrate, wherein all of the plurality of contacts is coplanar with the ledge, and none of the plurality of first solder bumps are coplanar with the ledge, and wherein an upper surface of each of the plurality of first solder bumps are essentially aligned with an upper surface of each of the

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plurality of contacts on a surface of the second substrate opposing the first substrate.

59. The semiconductor structure of 55, wherein the plurality of contacts comprise a plurality of second solder bumps each having a volume smaller than a volume of each of the plurality of first solder bumps.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35

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U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi.

Nishiguchi does not appear to explicitly teach the following:

10. The semiconductor structure according to 1, wherein the contacts each have a diameter of less than about 50  $\mu\text{m}$ .
11. The semiconductor structure according to 1, wherein the contacts each have a diameter of about 10  $\mu\text{m}$ .
12. The semiconductor structure according to 1, wherein the contacts each have a diameter of less than about 10  $\mu\text{m}$ .
13. The semiconductor structure according to 1, wherein the contacts have a pitch of less than about 100  $\mu\text{m}$ .
14. The semiconductor structure according to 1, wherein the contacts have a pitch of about 30  $\mu\text{m}$ .
15. The semiconductor structure according to 1, wherein the contacts have a diameter about 20% of the diameter of the first solder bumps.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose these particular dimensions because applicant has not



disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishiguchi as applied to claims 1, 3-6, 17, 18, 20, 25, 54-57 and 59, and further in combination with Lin (3871015).

Nishiguchi does not appear to explicitly teach the following:

2. The semiconductor structure according to 1, wherein the contacts have a different composition than the first solder bumps.

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16. The semiconductor structure according to 1, wherein the contacts comprise a material having a higher melting point than the first solder bumps.

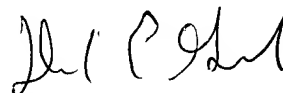
Nonetheless, at column 4, lines 6-18; and column 5, line 30 to column 6, line 13, Lin teaches a semiconductor structure wherein contacts 104, 106 have a different composition than first solder bumps 100, 102 and comprise a material having a higher melting point than the first solder bumps.

Moreover, it would have been obvious to combine the product of Lin with the product of Nishiguchi because it would reduce structure stress.

***Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to the group receptionist whose telephone number is 703-308-1782.***

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (703) 308-2947. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is 703/305-3431.



David E. Graybill  
Primary Examiner  
Art Unit 2814

D.G.  
6-Dec-01